**EEE2001 Digital Electronics Design**

**Swinburne University of Technology (Sarawak Campus)**

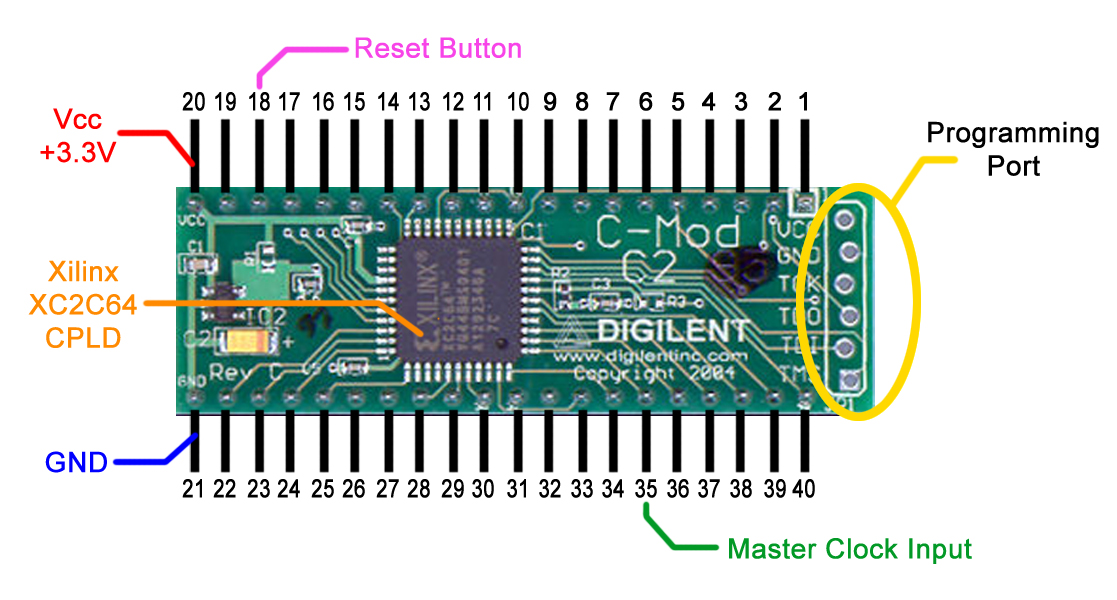
***Digilent C-Mod C2 Wiring Manual***

**Introduction**

The Digilent C-Mod C2 board is a DIP breakout board for Xilinx XC2C64 CPLD for easy prototyping with breadboards where the use of small surface mount package is impractical.

**Connecting C-Mod C2 to Breadboard**

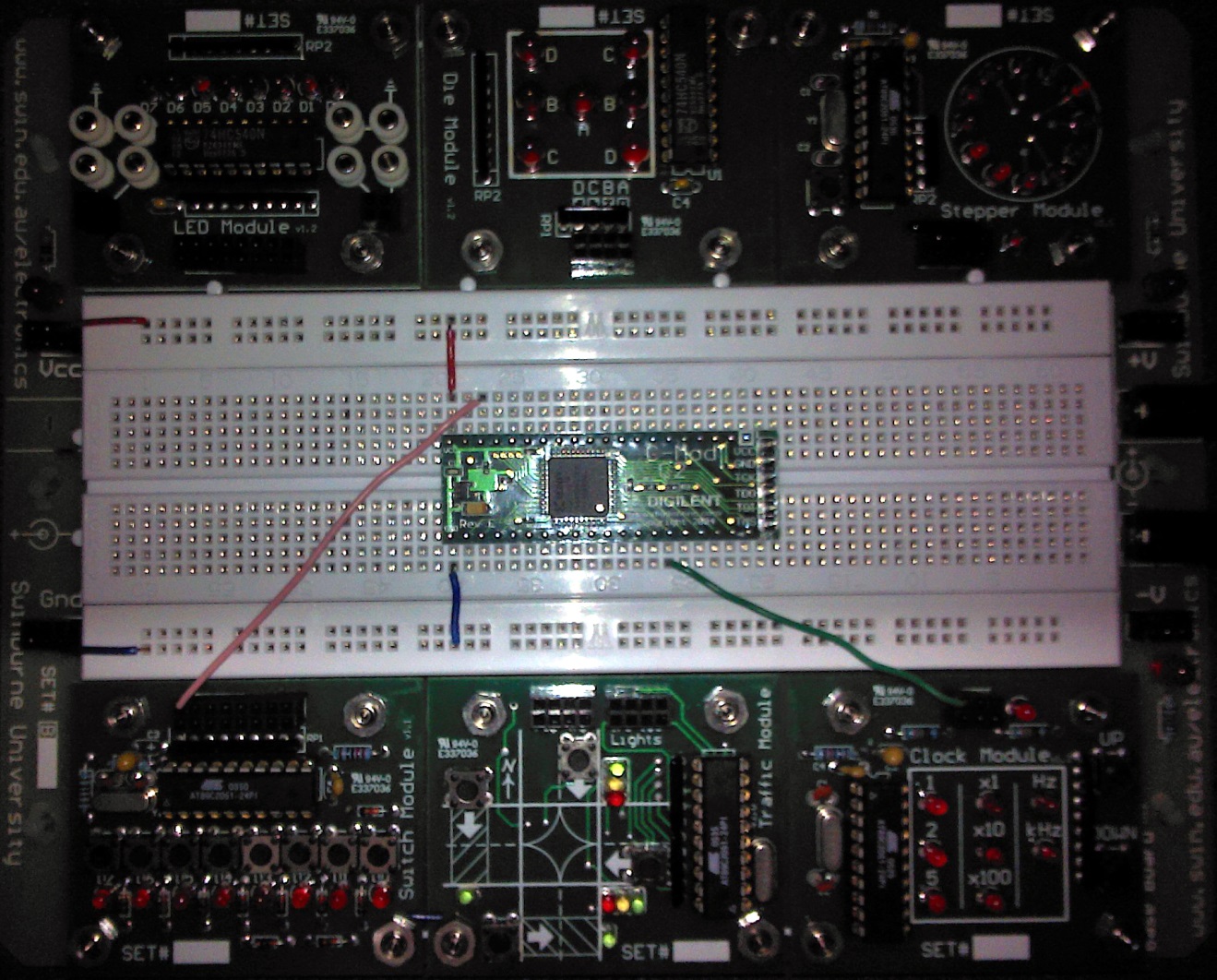
The pin numbering of C-Mod C2 board (together with important pins to be connected) is shown in the figure below.



**Figure 1 Digilent C-Mod C2 Pin Connection**

**There are few important points to be noted:**

* Do not change any wiring while the circuitry has its power on.
* All connections have to be made correctly and checked properly before turning on the power. The most important pins that should never be connected wrongly are Vcc and GND!!
* It is highly recommended that you follow the wiring on Figure 2. This wiring is used for all your VHDL experiments (including introduction session and your VHDL Project) in this unit. Once you have done this wiring, you do not need to dismantle it until you have finished and demonstrated the VHDL Project.



**Figure 2 Basic Digilent C-Mod C2 Pin Connections on the baseboard**

* The connections made as seen in Figure 2 are:

|  |  |
| --- | --- |
| **Name** | **Description** |
| Vcc (Red) | This is the +3.3V supply to the Xilinx XC2C64 CPLD |
| GND (Blue) | This is the ground of the voltage supply |
| Master Clock Input (Green) | This is the Master Clock input to the Xilinx XC2C64 CPLD. It should be connected to the output of the Clock Module. |
| Reset Button (Pink) | This is the reset button and should be connected to one of the outputs of the Switch Module |

**Table 1 List of connections to be made**

|  |  |  |
| --- | --- | --- |
| **C-Mod C2 Pin No.** | **Xilinx XC2C64 Pin No.** | **Type** |
| 1 | 12 | IO |
| 2 | 13 | IO |
| 3 | 14 | IO |
| 4 | 16 | IO |
| 5 |  |  |
| 6 |  |  |
| 7 |  |  |
| 8 |  |  |
| 9 | 18 | IO |
| 10 | 19 | IO |
| 11 | 20 | IO |
| 12 | 21 | IO |
| 13 | 22 | IO |
| 14 | 23 | IO |
| 15 | 27 | IO |
| 16 | 28 | IO |
| 17 | 29 | IO |
| 18 | 30 | GSR |
| 19 |  |  |
| 20 | 15 | VCC |
| 7,26 | VCCIO |
| 35 | VAUX |
| 21 | 4,17,25 | GND |
| 22 | 31 | GTS2 |
| 23 | 32 | GTS3 |
| 24 | 33 | GTS0 |
| 25 | 34 | GTS1 |
| 26 | 36 | IO |
| 27 | 37 | IO |
| 28 | 38 | IO |
| 29 | 39 | IO |
| 30 | 40 | IO |
| 31 | 41 | IO |
| 32 | 42 | IO |
| 33 | 43 | GCK0 |
| 34 | 44 | GCK1 |
| 35 | 1 | GCK2 |
| 36 | 2 | IO |
| 37 | 3 | IO |
| 38 | 5 | IO |
| 39 | 6 | IO |
| 40 | 8 | IO |

**Table 2 Pin Mapping between C-Mod C2 and Xilinx XC2C64**

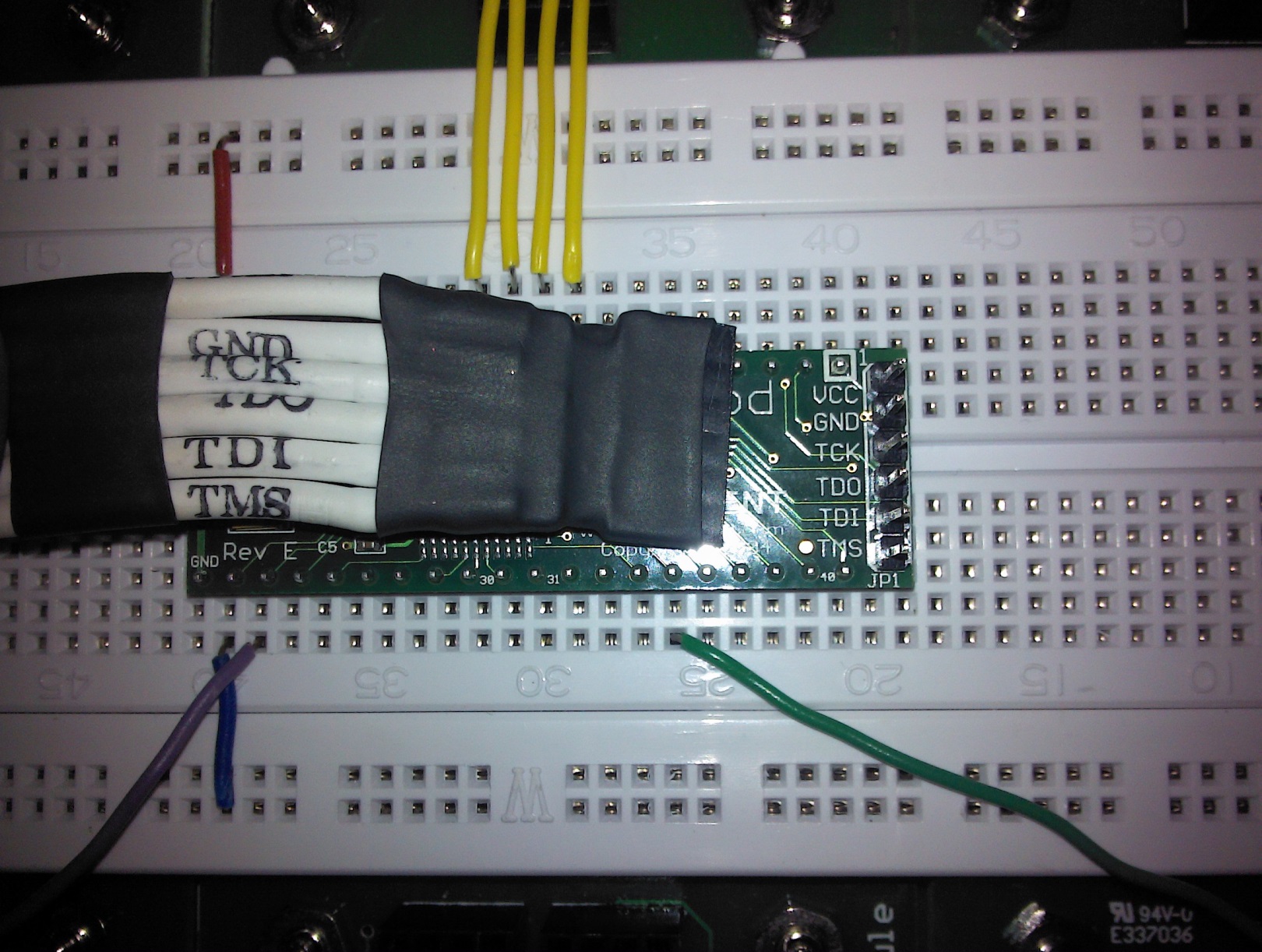
**Connecting the USB-JTAG Programmer to C-Mod C2**

The USB-JTAG Programmer is the device to load the bit file generated by the Xilinx ISE to the Xilinx CPLD. Follow these instructions in order to complete the connection from USB-JTAG to C-Mod C2:

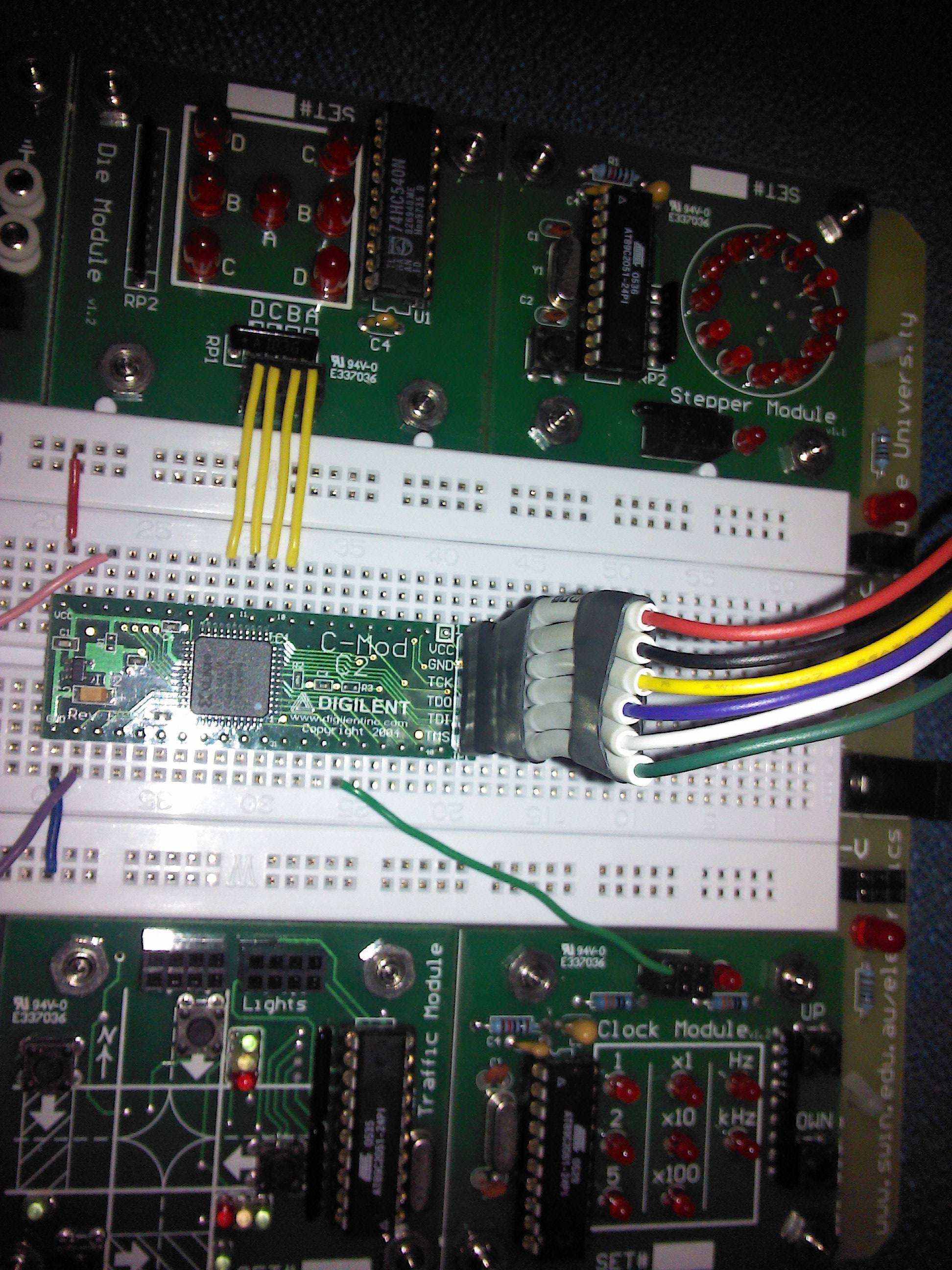
* The USB-JTAG driver has to be installed in the computer before the Xilinx ISE recognizes it as a valid programming device. The driver is included in the Digilent Adept 2 software, which can be downloaded from:

<http://www.digilentinc.com/Data/Products/adept2/digilent.adept.system_v2.9.4.exe>

* Connect the USB-JTAG to USB port of the PC. If the driver is not installed, the Found New Hardware Wizard will pop out and ask for the driver search option.
* Select *Install from a specific location (Advanced)*
* Click *Next*
* Select *Include this location in the search >*  *Browse*
* Browse to *C:\Program Files\Digilent\Runtime\UsbDriver\i386* directory.
* The wizard will then install the required driver.
* After installing the driver, plug in the other end of USB-JTAG (the end with four wires) into the programming port of the C-Mod C2 (see Figure 3 and Figure 4). This connection should not be connected backwards. Confirm your connection by checking the labels on the USB-JTAG cable and the C-Mod C2 Board. There are six wires on the connector plug:
  1. VREF (VCC on C-Mod C2)
  2. GND
  3. TCK
  4. TDO
  5. TDI
  6. TMS



**Figure 3 USB-JTAG programming cable and the C-Mod C2 Programming Port**



**Figure 4 The correct connection between USB-JTAG and C-Mod C2**



**Figure 5 Schematic of C-Mod C2**